



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,484	01/20/2004	Timothy Henson	IR-2364	2919
2352	7590	03/14/2005	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			ERDEM, FAZLI	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/761,484	HENSON, TIMOTHY	
	<b>Examiner</b>	<b>Art Unit</b>	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 13 December 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-17 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Hurkx et al. (6,541,817) in view of Hadizad et al. (6,756,273) further in view of Ahlers et al. (6,667,514).

Regarding Claims 1-12, Hurkx et al. disclose a trench-gate semiconductor devices and their manufacture where in Fig. 1 it is disclose a semiconductor region of 14 formed over substrate, a semiconductor trench receiving region 10 formed over the semiconductor region 14, plurality of trenches 20 formed in the trench receiving region, each treanch including a bottom surface and sidewalls 20b, conductive material 61 and 62 formed inside the trenches, channel region 15 between the trenches, gate electrode 11, dielectric material 17 formed inside the trenches. Hurkx et al. fail to disclose drain column regions directly below the trench and the required charge balancing structure. However, Hadizad et al. disclose a semiconductor component and method of manufacturing where in Figs. 9-12, element 326 is a drain column an is directly below the trench 326. Furthermore, Ahlers et al. disclose a semiconductor component with charge compensation structure and associated fabrication where in Fig. 8A, regions SP are charge balancing regions.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required drain column region directly below the trench and the required charge balancing structure in Hurkx et al. as taught by Hadizad et al. and Ahlers et al., respectively, in order to have a power semiconductor structure with increased performance.

3. Claims 13-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Hurkx et al. (6,541,817) in view of Darwish (2003/0102564) further in view of Ahlers et al. (6,667,514).

Regarding Claims 13-17, Hurkx et al. disclose a trench-gate semiconductor devices and their manufacture where in Fig. 1 it is disclose a semiconductor region of 14 formed over substrate, a semiconductor trench receiving region 10 formed over the semiconductor region 14, plurality of trenches 20 formed in the trench receiving region, each treanchn including a bottom surface and sidewalls 20b, conductive material 61 and 62 formed inside the trenches, channel region 15 between the trenches, gate electrode 11, dielectric material 17 formed inside the trenches. Hurkx et al. fail to disclose the required drain column under the trench and the method, and the required charge balancing structure. However, Darwish discloses a trench MOSFET having implanted drain-drift region and process for manufacturing the same where the required drain column region is under the trench as shown in Fig. 18 and method are disclosed. Furthermore, Ahlers et al. disclose a semiconductor component with charge compensation structure and associated fabrication where in Fig. 8A, regions SP are charge balancing regions.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required drain column below trench and method

Art Unit: 2826

and the required charge balancing structure in Hurkx et al. as taught by Darwish and Ahlers et al. respectively in order to manufacture a power semiconductor structure with increased performance.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 3, 2005  
FE

NATHAN J. FLYNN  
EXAMINER  
TECHNOLOGY CENTER 2800